What is claimed is:

1. A semiconductor test apparatus that tests the operation of a semiconductor based on a plurality of pattern data, comprising:

a counter device that counts the number of times pattern data is used for each of said pattern files; and

a control unit that produces a pattern file use frequency table showing the relationship between each of said files and said number of times the files are used, and stores this pattern file use frequency table in the memory.

2. A semiconductor test apparatus according to claim 1 wherein said counting device counts the number of times said pattern data is used in a set of test for a predetermined number of semiconductors.

3. A semiconductor test according to claim 1, wherein said control unit rearrange the pattern files in descending order of frequency of use based on said pattern file use frequency table after producing said pattern file use frequency table.

4. A semiconductor test apparatus according to claim 1, wherein said control unit deletes the pattern files in ascending order of frequency of use in the case that the capacity of the executive memory is insufficient when transferring said pattern files to the executive memories.

5. A control method of the semiconductor test apparatus that tests the operation of a semiconductor based on a plurality of pattern data, comprising the steps of:

counting the number of times said pattern data is used for each pattern file; and preparing a pattern file use frequency table that shows the relationship between each file and the number of times these files are used, and storing this pattern file use frequency table in the memory.

6. A control method of the semiconductor test apparatus according to claim 5, wherein, in said counting step, the number of times said pattern data is used in a set of test for a predetermined number of semiconductors is counted.

7. A control method of the semiconductor test apparatus according to claim 5, wherein said storing step stores the pattern files in descending order of frequency of use based on said pattern file use frequency table after producing said pattern file use frequency table.

8. A control method of the semiconductor test apparatus according to claim 5, wherein said storage step deletes the pattern in ascending order of frequency of use in the case that the capacity of the executive memory is insufficient when transferring said pattern files to the executive memories.